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EXAMINER
KENNEDY, JENNIFER M

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 11/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/635,811	PARK ET AL.	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

In view of Applicants' amendment to the specification, the drawing objection is withdrawn.

In view of Applicants' amendments to claims 2 and 4, the objections to these claims are withdrawn.

The examiner notes that the Terminal Disclaimer filed August 9, 2004 was disapproved. However, in light of the amendments to the claims, the Double Patenting rejection is withdrawn.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 recites the limitation "the silicon nitride" in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim. The examiner notes that a first silicon nitride layer and a second silicon nitride layer are recited in claim 1. It is unclear to the examiner which silicon nitride layer, the first or the second, is being formed in this manner. The examiner believes that applicant intended on reciting the

first silicon nitride layer because claim 5 depends on claim 4, which refers to the method of forming the silicon nitride layer in step (c), which correlates to the step of forming the first silicon nitride layer. The examiner will examine accordingly.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al. (U.S. Patent No. 6,350,707) in view of Weimer (U.S. Patent Appl. 2003/0042526).

In re claim Liu et al. discloses the method for fabricating a capacitor of a semiconductor device comprising the steps of:

(a) forming a conductive silicon layer for a bottom electrode (102) on a substrate (100);

(b) forming a first silicon oxide layer (104) on the conductive silicon layer;

(c) forming a first silicon nitride layer (106) on the first silicon oxide layer ;

(d) forming a second silicon oxide layer (108) on the first silicon nitride layer;

(e) forming a second silicon nitride layer (106) on the second silicon oxide layer;

(f) forming a dielectric layer (108, see Figure 1D and column 3, lines 1-9) on the second silicon nitride layer.

Liu et al. does not disclose the method of forming a top electrode on the dielectric layer. Weimer discloses the method of forming a top electrode on a dielectric layer (see [0034]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a top electrode on the dielectric layer because as Weimer teaches ([0034]) it allows for the completion of the capacitor.

In re claim 2, Liu et al. disclose the method wherein in the step (d) a native oxide layer (108) is used. The examiner notes that the applicants have defined a native oxide to be an oxide generated wherein the substrate is exposed in an atmosphere (see specification, page 7, lines 15-23). The examiner notes that Liu et al discloses the substrate exposed in an atmosphere of nitric oxide or nitrogen monoxide (see column 2, lines 40-43).

In re claim 3, the combined Liu et al. and Weimer do not disclose the method wherein the native oxide layer is formed in a thickness ranging from about 1 angstrom to about 5 angstroms. Liu et al. discloses the method of forming a thin native oxide layer (see column 2, lines 25-35).

The examiner notes that Applicant does not teach that the claimed thickness range solve any stated problem or are for any particular purpose. Therefore, the thickness range lacks criticality in the claimed invention and does not produce unexpected or novel results. Thus, it would have been obvious to one of ordinary skill in

the art at the time the invention was made to form a silicon oxide with a thickness of 1 angstrom to about 5 angstroms, since the invention would perform equally well when the silicon oxide is formed at different thicknesses to form a silicon oxide dielectric layer that prevents a short circuit, prevents leakage current, and is thin to allow for a high capacitance device, and because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

In re claim 4 and 5, Liu et al. disclose the invention as claimed and rejected above, including the method wherein in step (c), a thermal treatment process is carried out in an atmosphere of NH_3 gas, and wherein the silicon nitride layer is formed by using a source of dicholorosilane (DCS) in an atmosphere of NH_3 gas (see column 2, lines 34-40).

Liu et al. do not explicitly disclose the method wherein the thermal treatment process is carried out at a pressure ranging from about 10 Torr to about 100 Torr and the silicon nitride layer is formed at a pressure ranging from about 1 Torr to about 10 Torr.

The examiner notes that Applicant does not teach that the claimed pressure ranges solve any stated problem or are for any particular purpose. Therefore, the pressure ranges lack criticality in the claimed invention and do not produce unexpected or novel results. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform a thermal treatment process at a pressure

ranging from about 10 Torr to about 100 Torr and forming the silicon nitride layer at a pressure ranging from about 1 Torr to about 10 Torr, since the invention would perform equally well whether the deposition of the silicon nitride is performed at different pressures to allow for a reaction to form a silicon nitride dielectric layer that allows for a lower leakage current for the device, (see Liu et al., column 2, lines 34-55) and because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

In re claim 6, Liu et al. does not disclose the method wherein the dielectric layer is comprised of a material having one of a high dielectric constant and being a ferroelectric substance. Weimer discloses the method wherein the dielectric layer is comprised of a material having one of a high dielectric constant and being a ferroelectric substance (see paragraph [0031]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the last oxide layer of the ONONO or ONONONO layers with a high K dielectric of Weimer in order to allow for a higher capacitance, with the added benefits of a diffusion as discussed by Weimer, in paragraphs [0031]-[0033])

In re claim 7, Weimer discloses the method wherein the dielectric layer is selected from a group of Ta_2O_5, Al_2O_3, HfO_2, BST, PZT, PBZT, and BLT (see paragraph [0031]).

In re claim 9, Weimer discloses the method of performing thermal treatment process for improving device characteristics and crystallization of the dielectric layer after the step (f) (see [0032-0033]).

Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al. (U.S. Patent No. 6,350,707) in view of Huanga et al. (U.S. Patent No. 5,670,431)

In re claim Liu et al. discloses the method for fabricating a capacitor of a semiconductor device comprising the steps of:

(a) forming a conductive silicon layer for a bottom electrode (102) on a substrate (100);

(b) forming a first silicon oxide layer (104) on the conductive silicon layer;

(c) forming a first silicon nitride layer (106) on the first silicon oxide layer ;

(d) forming a second silicon oxide layer (108) on the first silicon nitride layer;

(e) forming a second silicon nitride layer (106) on the second silicon oxide layer;

(f) forming a dielectric layer (108, see Figure 1D and column 3, lines 1-9) on the second silicon nitride layer.

Liu et al. does not disclose the method of forming a top electrode on the dielectric layer. Huanga et al. disclose the method of forming a top electrode on a dielectric layer (42). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a top electrode on the dielectric to allow for the completion of the capacitor.

In re claim 2, Liu et al. disclose the method wherein in the step (d) a native oxide layer (104) is used. The examiner notes that the applicants have defined a native oxide to be an oxide generated wherein the substrate is exposed in an atmosphere (see specification, page 7, lines 15-23). The examiner notes that Liu et al discloses the substrate exposed in an atmosphere of nitric oxide or nitrogen monoxide (see column 2, lines 40-43).

In re claim 3, Liu et al. does not disclose the thickness of the native oxide layer. Huanga et al. teaches a thickness ranging from about 1 angstrom to about 5 angstroms for the native oxide thickness of a ON layer (see column 6, lines 18-30). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the native oxide thickness ranging from about 1 angstrom to about 5 angstroms to allow for a ultra thin integrate dielectric film for a capacitor (see Huanga et al., column 6, lines 18-55).

In re claim 4 and 5, both Liu et al. and Huanga et al. disclose the invention as claimed and rejected above, including the method wherein in step (c), a thermal treatment process is carried out in an atmosphere of NH_3 gas, and wherein the silicon nitride layer is formed by using a source of dicholorosilane (DCS) in an atmosphere of NH_3 gas (see column 2, lines 34-40 or Liu et al.; see column 3, lines 5-13, column 6, lines 9-16, column 6, lines 31-41 of Huanga et al.).

Neither Liu et al. nor Huanga et al. do not explicitly disclose the method wherein the thermal treatment process is carried out at a pressure ranging from about 10 Torr to

about 100 Torr and the silicon nitride layer is formed at a pressure ranging from about 1 Torr to about 10 Torr.

The examiner notes that Applicant does not teach that the claimed pressure ranges solve any stated problem or are for any particular purpose. Therefore, the pressure ranges lack criticality in the claimed invention and do not produce unexpected or novel results. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the thermal treatment process at a pressure ranging from about 10 Torr to about 100 Torr and forming the silicon nitride layer at a pressure ranging from about 1 Torr to about 10 Torr, since the invention would perform equally well whether the nitridating occurs at different pressures and the deposition of the silicon nitride is performed at different pressures in order to form a uniform integrate silicon nitride/silicon oxide dielectric layer that prevents oxidation of the lower electrode, (see Huanga et al., column 7, lines 25-31) and because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

Claims 1 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al. (U.S. Patent No. 6,350,707) in view of Kizilyalli et al. (U.S. Patent Appl. 2002/0197790).

In re claim Liu et al. discloses the method for fabricating a capacitor of a semiconductor device comprising the steps of:

(a) forming a conductive silicon layer for a bottom electrode (102) on a substrate (100);

(b) forming a first silicon oxide layer (104) on the conductive silicon layer;

(c) forming a first silicon nitride layer (106) on the first silicon oxide layer ;

(d) forming a second silicon oxide layer (108) on the first silicon nitride layer;

(e) forming a second silicon nitride layer (106) on the second silicon oxide layer;

(f) forming a dielectric layer (108, see Figure 1D and column 3, lines 1-9) on the second silicon nitride layer.

Liu et al. does not disclose the method of forming a top electrode on the dielectric layer. Kizilyalli et al. discloses the method of forming a top electrode (17) on a dielectric layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a top electrode on the dielectric layer to allow for the completion of the capacitor.

In re claim 8, Liu et al. does not disclose the method of performing a thermal treatment process for densifying the first silicon oxide layer in order to minimize oxidation of the conductive silicon layer before any further deposition. Kizilyalli et al. discloses densifying a silicon oxide layer of a capacitor dielectric (see [0019-0023]) before any further deposition. It would have been obvious to one of ordinary skill in the art at the time the invention was made to densify a silicon oxide layer of a capacitor dielectric in order to improve the overall quality of the dielectric, remove traps in the layers and reduce the overall leakage through the dielectric layers (see [0021]). The examiner notes that densifying a silicon oxide layer would necessary minimize oxidation

of the layer below because as the density increases in the silicon oxide layer the space between atoms within the layer decreases, thus preventing atoms of oxygen from moving through the layer.

Response to Arguments

Applicant's arguments with respect to claims 1-7 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hazani (U.S. Patent No. 6,630,381) discloses the method of densifying a silicon oxide layer by a thermal process to prevent oxygen diffusion through it in subsequent steps (see column 10, lines 57-68).

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Kennedy
Patent Examiner
Art Unit 2812

jmk